Amendments to the Claims

Please cancel claims 8-10 and claims 16-19 without prejudice.

The following listing of claims will replace all prior versions and/or listings of claims in the application.

Listing of Claims:

1. (previously presented): A semiconductor device, comprising:

a silicon body, in which are formed source and drain regions defining between them a channel region;

a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and

a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones.

2. (previously presented): The device of claim 1, wherein the buried dielectric layer extends between the source and drain regions.

3. (previously presented): The device of claim 1, wherein the buried dielectric layer extends over the entire surface of the silicon body below the source and drain regions.

4. (previously presented): The device of claim 1, wherein the device has a planar structure.

5. (previously presented): The device of claim 1, wherein the buried dielectric layer is an air-filled cavity.

6. (previously presented): The device of claim 1, wherein the buried dielectric layer is a solid material.

7. (previously presented): The device of claim 1, wherein the device is a transistor.

8-10. (cancelled)

11. (previously presented): The device of claim 1, wherein the buried dielectric layer has a thickness between about 1 nm and about 50 nm.

12. (previously presented): The device of claim 1, wherein the thin silicon layer has a thickness between about 1 nm and about 50 nm.

13. (previously presented): The device of claim 1, wherein a length of the two opposed zones is less than about 100 nm.

14. (previously presented): The device of claim 1, wherein the thin gate dielectric layer comprises SiO_2.

15. (previously presented): The device of claim 1, wherein the source and drain regions lie in the same plane as the gate.

16-19. (cancelled)

20. (previously presented): A semiconductor device, comprising:

a silicon body, in which are formed source and drain regions defining between them a channel region;

a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and

a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones, and wherein the buried dielectric layer extends between the source and drain regions.

21. (new): A method for manufacturing a semiconductor device, comprising:

forming, in a silicon body, source and drain regions defining between them a channel region;

providing a thin gate dielectric layer on the channel region and a gate on the thin gate dielectric layer; and

providing a buried layer of a dielectric and a thin silicon layer extending between the source and drain regions and lying between the buried dielectric layer and the gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that the source and drain regions each overlap respectively, at least in part, one of said opposed zones.

22. (new): The method of claim 21, further comprising:

forming a germanium or SiGe alloy layer on a main surface of the silicon body;

forming the thin silicon layer on the germanium or SiGe alloy layer;

forming the thin gate dielectric layer on the thin silicon layer;

forming the gate on the gate dielectric layer and a hard mask on the gate;

forming first spacers on two opposed sides of the gate and of the hard mask, wherein the first spacers are made of a first material;

forming second spacers along the first spacers, wherein the second spacers are made of a second material different from the first material;

etching, on each side of the second spacers, of the gate dielectric layer, of the thin silicon layer, and optionally of part of the germanium or SiGe alloy layer;

selective etching of the germanium or SiGe alloy layer in order to form a tunnel;

optionally, filling the tunnel with the dielectric, wherein the dielectric is solid;

removing the second spacers in order to expose the two zones on the thin silicon layer, wherein the two zones are located respectively on either side of the first spacers; and

forming the source and drain regions on either side of the first spacers.

23. (new): The method of claim 22, wherein forming the source and drain regions comprises deposition of polycrystalline silicon by selective epitaxy in order to form polycrystalline silicon deposits on either side of the first spacers, wherein the polycrystalline silicon deposits are precursors of the source and drain regions and overlap, at least in part, the exposed zones of the thin silicon layer, and the method further comprising removing the gate hard mask and implanting a dopant in the polycrystalline silicon deposits in order to produce the source and drain regions.

24. (new): The method of claim 22, wherein forming the source and drain regions comprises deposition of a thick polycrystalline silicon encapsulating layer, forming a resin mask on the thick polycrystalline silicon layer, etching of the thick polycrystalline silicon layer to the desired shape and dimensions by means of the resin mask, removing of the resin mask, chemical-mechanical polishing of the thick silicon layer down to level with the gate in order to produce parts in the thick polycrystalline silicon layer which are intended to form the source and drain regions co-planar with the gate and implanting of a dopant in the parts in order to form the source and drain regions.

25. (new): The method of claim 22, wherein the SiGe alloy layer has a germanium fraction greater than about 0.1.

26. (new): The method of claim 22, wherein etching of the gate dielectric layer, of the thin silicon layer, or part of the germanium or SiGe alloy layer comprises plasma etching.

27. (new): The method of claim 22, wherein the first spacers comprise SiO_2 or Si_3N_4.

28. (new): The method of claim 22, wherein the second spacers comprise SiO_2 or Si_3N_4.